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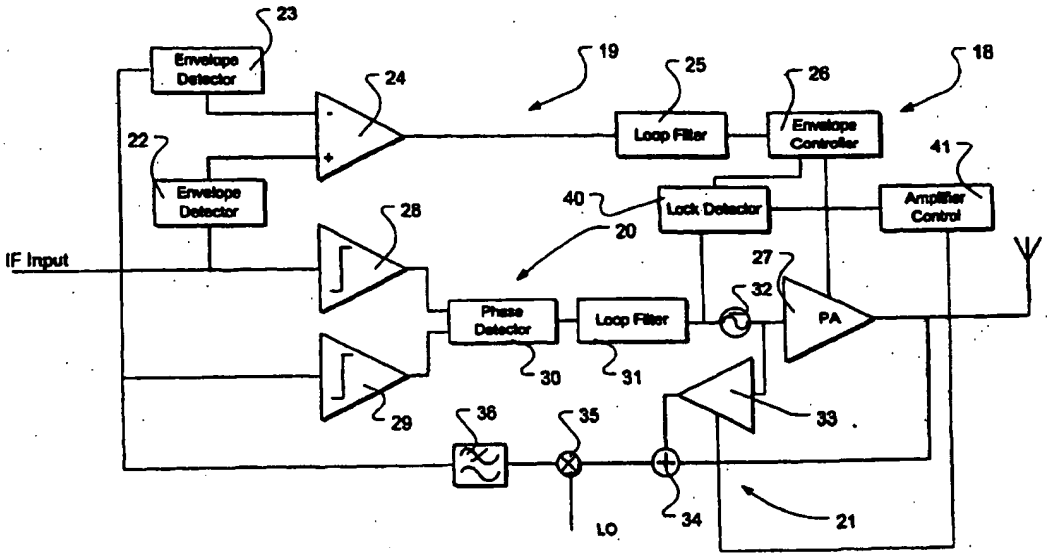
(54) Title: PHASE-LOCKED LOOP CIRCUIT



(57) Abstract: A phase-locked loop circuit has an output amplifier (27) and a main feedback path from the output of the output amplifier (27). A subsidiary feedback path is provided directly from the output of the circuit's VCO (32). At the start of operation, the output amplifier (27) is disabled and the subsidiary feedback path is used until lock is achieved. Then the output amplifier (27) is enabled and the main feedback loop is used. This avoids spurious outputs from the output amplifier while to loop locks.

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Phase-Locked Loop Circuit

Field of the Invention

The present invention relates to a phase locked loop circuit.

Background to the Invention

The present trend in portable communications devices such as mobile telephones is to increasingly lightweight devices with increased talk-time between battery recharge cycles. Such developments require ever more efficient radio-frequency (RF) amplifiers to minimise power consumption. In cellular systems such as GSM, the modulation scheme is a constant amplitude scheme, also referred to as constant envelope modulation, which permits use of efficient non-linear amplifiers. However, recent types of communication system such as EDGE and UMTS use non-constant envelope modulation schemes. The drawback is that the amplification of non-constant envelope RF signals requires the use of linear power amplifiers, which are inherently less efficient. The lower power efficiency of linear amplifiers translates into higher power consumption and higher heat dissipation.

A variety of linearisation architectures and schemes exist, including fixed and adaptive pre-distortion, adaptive bias, envelope elimination and restoration, polar loop and cartesian loop transmitters. Details of such devices are shown in "Increasing Talk-Time with Efficient Linear PA's", IEE Seminar on TETRA Market and Technology Developments, Mann S, Beach M, Warr P and McGeehan J, Institution of Electrical Engineers, 2000, which is incorporated herein by reference. However, many of these devices and techniques are unsuitable for battery operated portable devices such as mobile telephones, or are incapable of meeting current RF design standards, such as the TETRA linearity standard, ETSI publication ETS 300 396-2; "Trans-European Trunked Radio (TETRA); - Voice plus Data (V+D) – Part 2: Air Interface (AI)"; March 1996.

Envelope elimination and restoration (EER) transmitters separate envelope and phase information from an input modulated signal. The phase information is then passed through a power amplifier as a constant envelope signal, permitting the use

of efficient, non-linear amplifiers, while the envelope signal is added to the power amplifier output. In order to correct AM-PM distortion, phase feedback is employed and the power amplifier is effectively placed within phase-locked loop.

A problem arises in the spurious emissions are generated by the power amplifier in the period before the loop is locked at the beginning of a transmission.

Summary of the Invention

According to the present invention, there is provided a phase-locked loop circuit comprising an oscillator controlled in dependence on the output of a phase detector, an output amplifier for amplifying the output of the oscillator and a feedback path to the phase detector from the output of the output amplifier, characterised by a second feedback path from the output of the oscillator to the phase detector, by-passing the output amplifier, and control means for disabling the output amplifier when the loop circuit is not locked and interrupting the second feedback path when the loop circuit has become locked.

Thus, unwanted components in the output of the output amplifier can be avoided by ensuring that the amplifier does not become active until the loop has achieved lock.

Preferably, the second feedback path includes a variable gain amplifier, the control means being configured to interrupt the second feedback path by reducing the gain of the variable gain amplifier. More preferably, the control means is configured to interrupt the second feedback path by ramping down the gain of the variable gain amplifier. Still more preferably, the control means is configured to ramp up the gain of output amplifier on enabling thereof, the ramping down of the gain of the variable gain amplifier overlapping the ramping up of the gain of output amplifier. Phase control means may be included for matching the phase of the output of the variable gain amplifier to that of the output of the output amplifier when both are operating. Such phase control means may comprise a variable delay in the second feedback path, a phase detector receiving a signal from the second feedback path downstream of the variable delay and a signal from the first feedback path and a

low-pass filter for filtering the output of the phase detector to provide a delay control input signal for the variable delay.

Preferably, the first and second feedback paths share a common portion. More preferably, the first and second feedback paths are united by a summer and/or the common portion includes a frequency down converter.

A circuit according to the present invention may be advantageously employed in an envelope elimination and restoration transmitter such that the first feedback path provides a feedback signal for a closed loop envelope restoration circuit and the control means includes an envelope controller for controlling the gain of the output amplifier.

A circuit according to the present invention may be advantageously employed in a mobile phone such that the output amplifier is an RF power amplifier.

Brief Description of the Drawings

Figure 1 is a perspective view of a mobile telephone handset;
Figure 2 is a schematic diagram of mobile telephone circuitry for use in the telephone handset of Figure 1;
Figure 3 is a block diagram of a first embodiment of the present invention;
Figure 4 illustrate the initiation of a transmission by the embodiment shown in Figure 3; and
Figure 5 is a block diagram of a second embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Embodiments of the invention will now be described by way of example with reference to the accompanying drawings.

Referring to Figure 1, a mobile station in the form of a mobile telephone handset 1 includes a microphone 2, keypad 3, with soft keys 4 which can be programmed to perform different functions, an LCD display 5, a speaker 6 and an antenna 7 which is contained within the housing.

The mobile station 1 is operable to communicate through cellular radio links with individual public land mobile networks (PLMNs) operating according to communication schemes such as UMTS and EDGE.

Figure 2 illustrates the major circuit components of the telephone handset 1. Signal processing is carried out under the control of a digital micro-controller 9 which has an associated flash memory 10. Electrical analogue audio signals are produced by microphone 2 and amplified by pre-amplifier 11. Similarly, analogue audio signals are fed to the speaker 6 through an amplifier 12. The micro-controller 9 receives instruction signals from the keypad and soft keys 3, 4 and controls operation of the LCD display 5.

Information concerning the identity of the user is held on a smart card 13 in the form of a GSM SIM card which contains the usual GSM international mobile subscriber identity (IMSI) and an encryption key K_i that is used for encoding the radio transmission in a manner well known per se. The SIM card is removably received in a SIM card reader 14.

The mobile telephone circuitry includes a codec 15 and an rf stage 16 including a power amplifier stage 17 feeding the antenna 7. The codec 15 receives analogue signals from the microphone amplifier 11, digitises them into an appropriate signal format and feeds them to the power amplifier stage 17 in the rf stage 16 for transmission through the antenna 7 to the PLMN shown in Figure 1. Similarly, signals received from the PLMN are fed through the antenna 7 to be demodulated in the rf stage 16 and fed to codec 15, so as to produce analogue signals fed to the amplifier 12 and speaker 6.

Referring to Figure 3, the power amplifier stage 17 comprises an envelope elimination and restoration (EER) transmitter 18 which separates the envelope and phase components of an input modulated IF signal into two separate forward paths 19, 20. A common feedback path 21 is used for control of both the envelope and phase components of the RF output by the amplifier stage 17.

The envelope forward path 19 comprises first and second envelope detectors 22, 23 which detect the envelopes of the input modulated IF signal and the feedback signal from the feedback path 21 respectively. The outputs of the envelope detectors 22, 23 are fed to respective inputs of a comparator 24. The output of the comparator 24 is filtered by a low-pass filter 25 and applied to an envelope controller 26.

The envelope controller 26 comprises a fast power supply modulator which directly modulates the supply voltage of the power amplifier 27 itself.

The phase forward path 20 comprises first and second limiters 28, 29 which limit the input modulated IF signal and the feedback signal respectively to produce respective constant-amplitude signals. The constant amplitude signals are applied to a phase detector 30 and the output of the phase detector 30 is filtered by a low-pass filter 31 and applied to a voltage-controlled oscillator 32 as is conventional in a phase-lock loop. The RF signal produced by the voltage-controlled oscillator 32 is input into the power amplifier 27 which amplifies it in dependence on the signal input to the envelope controller 26.

The output of the voltage-controlled oscillator 32 is also fed to a variable gain amplifier 33 which forms a branch of the common feedback path 21. A summer 34 receives the output of the variable gain amplifier 33 and the power amplifier 27 on respective inputs. The output of the summer 34 is connected to one input of a mixer 35. The other input of the mixer 35 receives a local oscillator signal. The output of the mixer is low-pass filtered by a feedback path filter 36 to select a low frequency mixing product. Thus, the mixer 35 and filter 36 act to down convert the RF output of the amplifier 27 to the IF signal frequency.

The output of the feedback path filter 36 is fed to the inputs of the second envelope detector 23 and the second limited 29 to complete the feedback paths of the envelope and phase control loops.

A lock detector 40 is provided to detect when the phase locked loop is locked. The lock detector 40 provides a control signal to the envelope controller 26 which disables the power amplifier 27 when the loop is not locked and enables the power amplifier 27 when the loop is locked.

The output of the lock detector 40 is also input into an amplifier control circuit 41 which produces a gain control signal for the variable gain amplifier 33. When the loop is not locked, the amplifier control circuit 41 outputs a circuit that keeps the variable gain amplifier's gain at a maximum. However, when lock is achieved and the output of the lock detector 40 changes state, the amplifier control circuit 41 outputs a signal that causes the gain of the variable gain amplifier 33 to decay to zero.

Referring to Figure 4, when a transmission is not being made, the power amplifier 27 is disabled and the voltage-controlled oscillator 32 runs freely, although it could also be disabled in the absence of an input IF signal.

When an IF signal is initially input, the voltage-controlled oscillator 32 is locked to the input IF signal by the action of the loop comprising the voltage-controlled oscillator 32, the variable gain amplifier 33, the mixer 35, the feedback path filter 36, the second limiter 29, the phase detector 30 and the low-pass filter 31. Since the power amplifier 27 is not producing an output, the summer 34 can be disregarded. During this period the frequency and phase of the voltage-controlled oscillator 32 vary until lock is achieved. Once lock has been achieved and the frequency and phase of the voltage-controlled oscillator 32 have stabilised, the output of the lock detector 40 changes state and the power amplifier 27 is enabled. The gain of the power amplifier 27 is ramped up to avoid sharp transitions in the output RF signal. While the gain of the power amplifier 27 is ramping up, the gain of the variable gain amplifier is ramped down by the amplifier control circuit 41 so that the feedback signal becomes dominated by the output of the power amplifier 27 and then completely dependent on the output of the power amplifier 27.

The gain of the variable gain amplifier 33 is ramped down while the gain of the power amplifier 27 is ramping up to ensure that the amplitude of feedback signal is always sufficient to be limited by the second limiter 29.

Referring to Figure 5, a second embodiment is substantially the same as the first embodiment, described above, except that a delay locked loop is added to the control the phase of the signal input to the variable gain amplifier 33. The delay locked loop is used so that during the transition from control on the basis of the voltage-controlled oscillator output to control on the basis of the power amplifier output, the output from the variable gain amplifier 33 does not tend to cancel the feedback from the power amplifier 27 due to a significant phase difference between the signals.

The delay locked loop comprises a voltage-controlled delay 37 for controllably delaying the output of the voltage-controlled oscillator 32 input into the variable gain amplifier 33, a phase detector 38 connected to receive the input to the variable gain amplifier 33 and the output of the power amplifier 27 as its inputs and a low-pass filter 39 for filtering the output of the phase detector 38 to provide a control signal for the voltage-controlled delay 37.

In another embodiment, the phase detector of the delay locked loop receives the outputs of the variable gain amplifier and the power amplifier as its inputs.

Claims

1. A phase-locked loop circuit comprising an oscillator (32) controlled in dependence on the output of a phase detector (30), an output amplifier (27) for amplifying the output of the oscillator (32) and a feedback path to the phase detector (30) from the output of the output amplifier (27), characterised by a second feedback path from the output of the oscillator (30) to the phase detector (30), by-passing the output amplifier (27), and control means (26, 40, 41) for disabling the output amplifier (27) when the loop circuit is not locked and interrupting the second feedback path when the loop circuit has become locked.

2. A circuit according to claim 1, wherein the second feedback path includes a variable gain amplifier (33), the control means (26, 40, 41) being configured to interrupt the second feedback path by reducing the gain of the variable gain amplifier (33).

3. A circuit according to claim 2, wherein the control means (26, 40, 41) is configured to interrupt the second feedback path by ramping down the gain of the variable gain amplifier (33).

4. A circuit according to claim 3, wherein the control means (26, 40, 41) is configured to ramp up the gain of output amplifier (27) on enabling thereof, the ramping down of the gain of the variable gain amplifier (33) overlapping the ramping up of the gain of output amplifier (27).

5. A circuit according to claim 4, including phase control means (37, 38, 39) for matching the phase of the output of the variable gain amplifier (33) to that of the output of the output amplifier (27) when both are operating.

6. A circuit according to claim 5, wherein the phase control means (37, 38, 39) comprises a variable delay (37) in the second feedback path, a phase detector (38) receiving a signal from the second feedback path downstream of the variable delay (37) and a signal from the first feedback path and a low-pass filter (39) for filtering

the output of the phase detector (38) to provide a delay control input signal for the variable delay (37).

7. A circuit according to any preceding claim, wherein the first and second feedback paths share a common portion.

8. A circuit according to claim 7, wherein the first and second feedback paths are united by a summer (34).

9. A circuit according to claim 7 or 8, wherein said common portion includes a frequency down converter (35, 36).

10. An envelope elimination and restoration transmitter including a circuit according to any preceding claim, wherein the first feedback path provides a feedback signal for a closed loop envelope restoration circuit, the control means (26, 40, 41) including an envelope controller (26) for controlling the gain of the output amplifier (27).

11. A mobile phone including a circuit according to any one of claims 1 to 9, wherein the output amplifier (37) is an RF power amplifier.

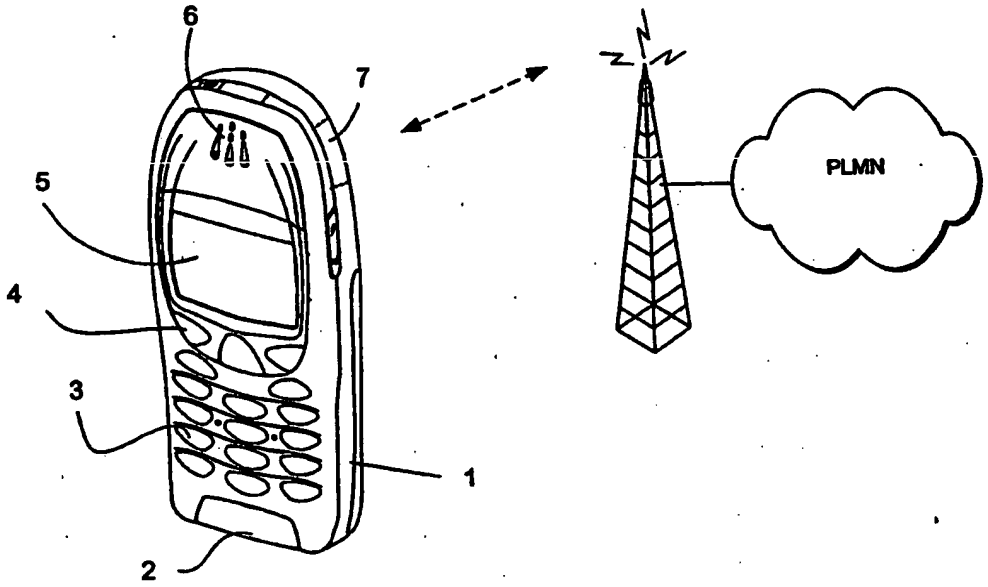

Figure 1

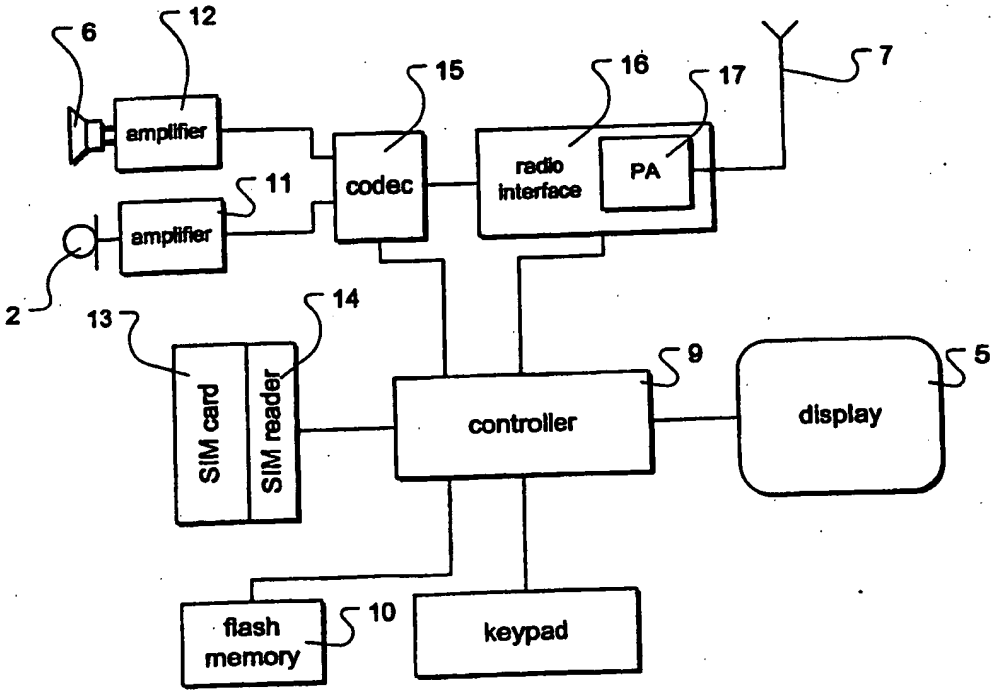

Figure 2

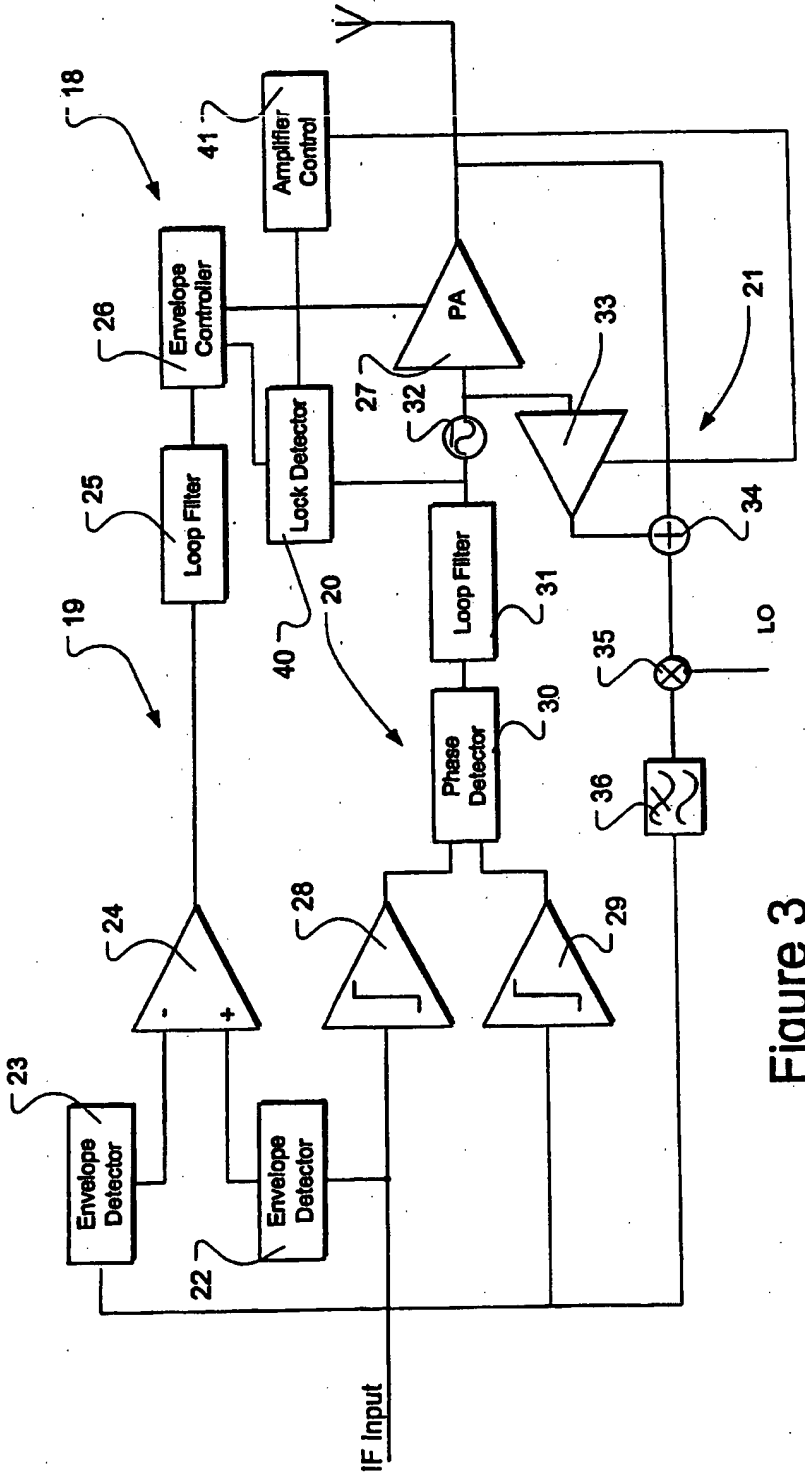
18
41
Amplifier Control
Envelope Controller
26
PA
27
32
33
21
Lock Detector
25
Loop Filter
34
20
40
Loop Filter
31
19
LO
35
Phase Detector
30
36
24
28
29
23
Envelope Detector
Envelope Detector
22
IF Input

Figure 3

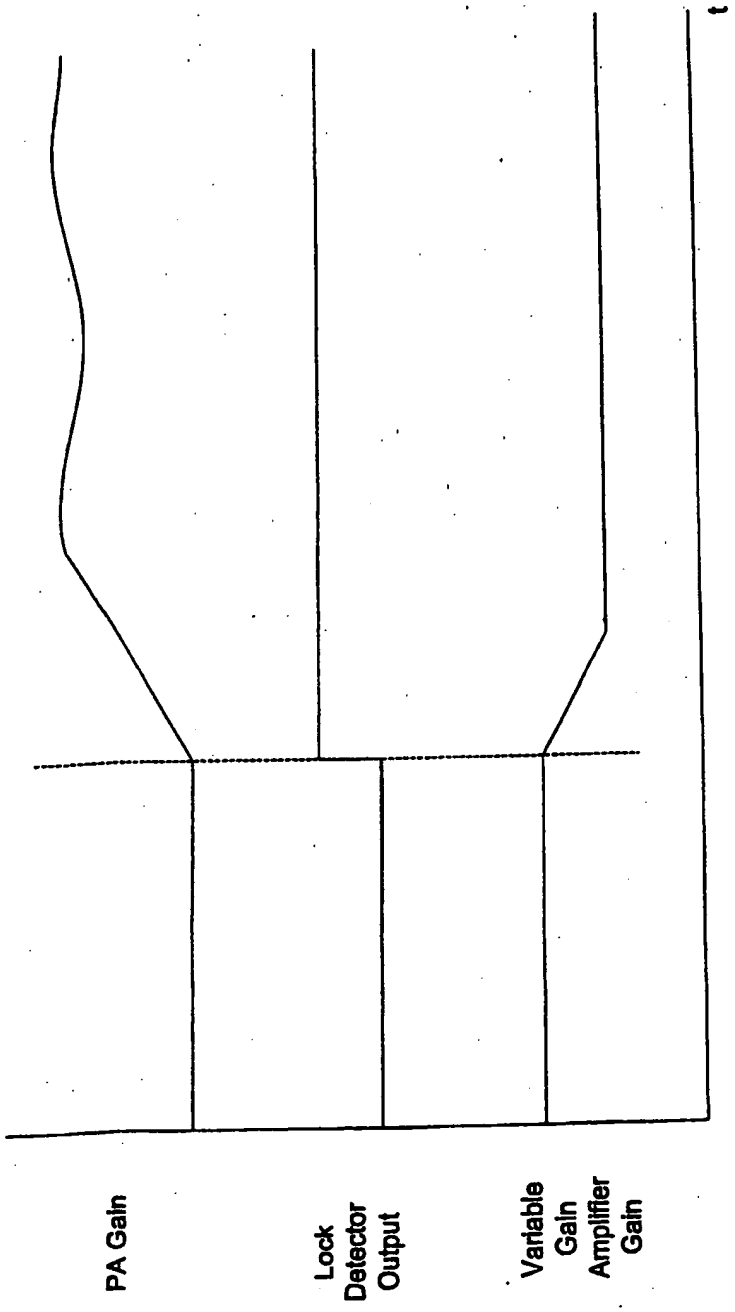

Figure 4

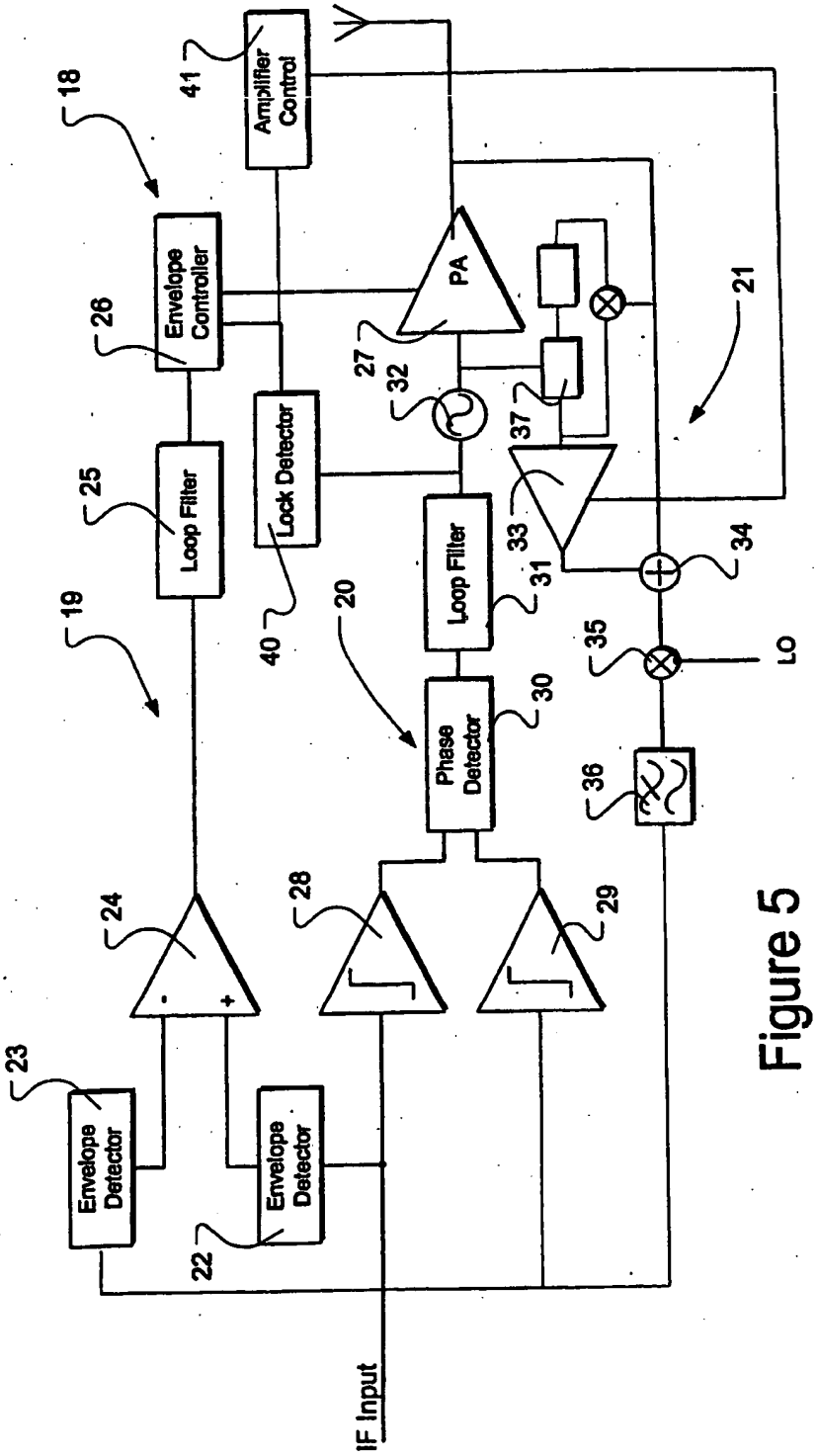

Figure 5

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 02/05722

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03L7/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L H03F H03L H03G H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 982 233 A (CARLSSON TORSTEN JOHN ET AL) 9 November 1999 (1999-11-09) column 4, line 37 -column 5, line 41; figure 3 column 6, line 52 -column 8, line 58; figure 6	1-11
A	EP 0 998 088 A (NOKIA MOBILE PHONES LTD) 3 May 2000 (2000-05-03) column 4, line 29 -column 5, line 35; figure 2	1-11
A	EP 1 052 770 A (SECURICOR WIRELESS TECHNOLOGY) 15 November 2000 (2000-11-15) *whole document*	1-11

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
20 May 2003	27/05/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax (+31–70) 340–3016	Aouichi, M

INTERNATIONAL SEARCH REPORT

Intern[redacted]nal Application No
P[redacted] 02/05722

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5982233 A	09-11-1999	SE 506841 C2	16-02-1998
		AU 724336 B2	14-09-2000
		AU 3468297 A	21-01-1998
		BR 9710043 A	10-08-1999
		CA 2259315 A1	08-01-1998
		DE 69717813 D1	23-01-2003
		EE 9800448 A	15-06-1999
		EP 0908004 A1	14-04-1999
		JP 2000513532 T	10-10-2000
		KR 2000016651 A	25-03-2000
		NO 985994 A	26-02-1999
		SE 9602585 A	29-12-1997
		WO 9800909 A1	08-01-1998
		TR 9802722 T2	22-03-1999
EP 0998088 A	03-05-2000	FI 982329 A	28-04-2000
		EP 0998088 A2	03-05-2000
		JP 2000138723 A	16-05-2000
		US 6480704 B1	12-11-2002
EP 1052770 A	15-11-2000	GB 2349994 A	15-11-2000
		EP 1052770 A1	15-11-2000
		JP 2001045079 A	16-02-2001